FIG. 1

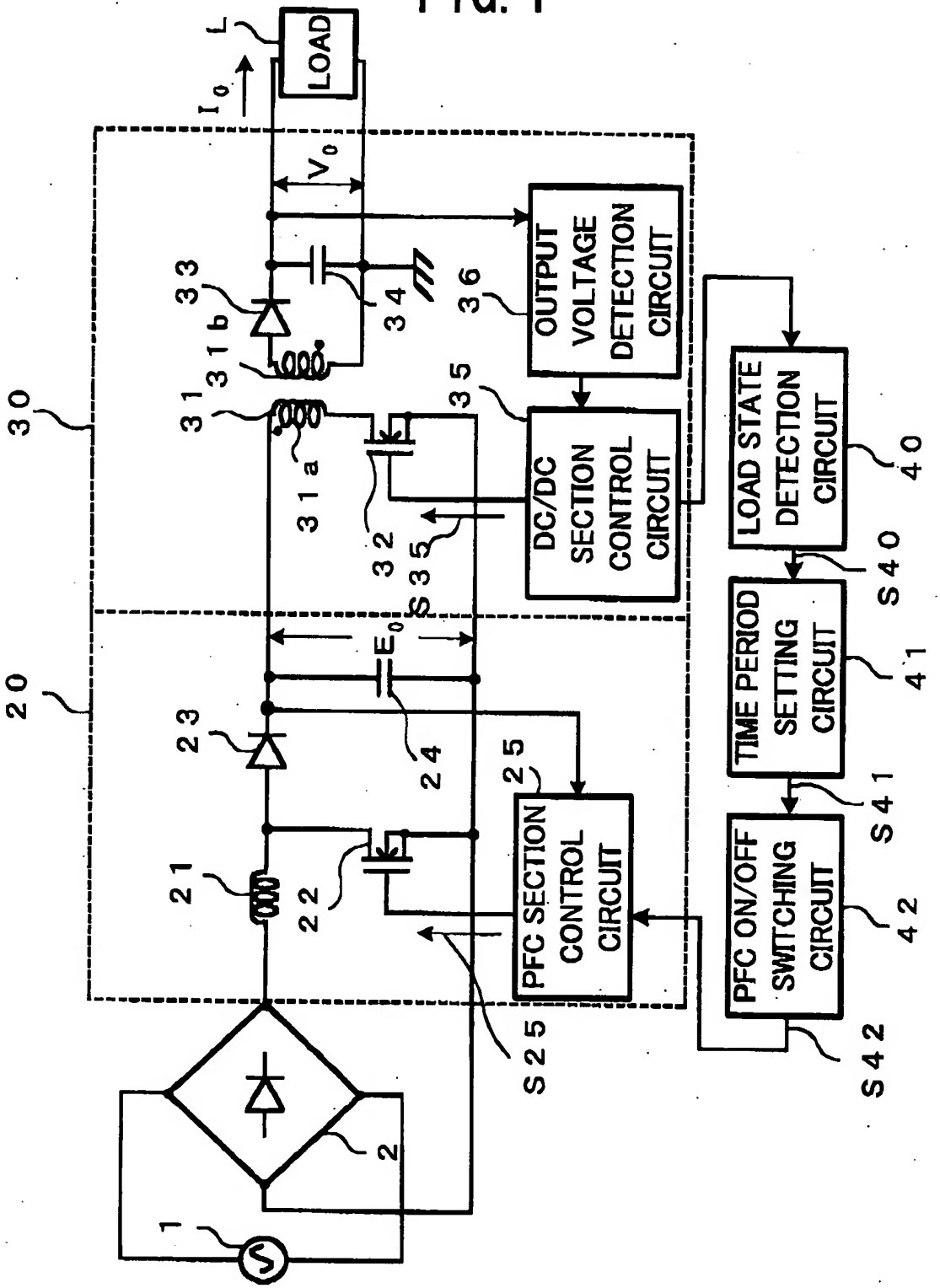

FIG.2

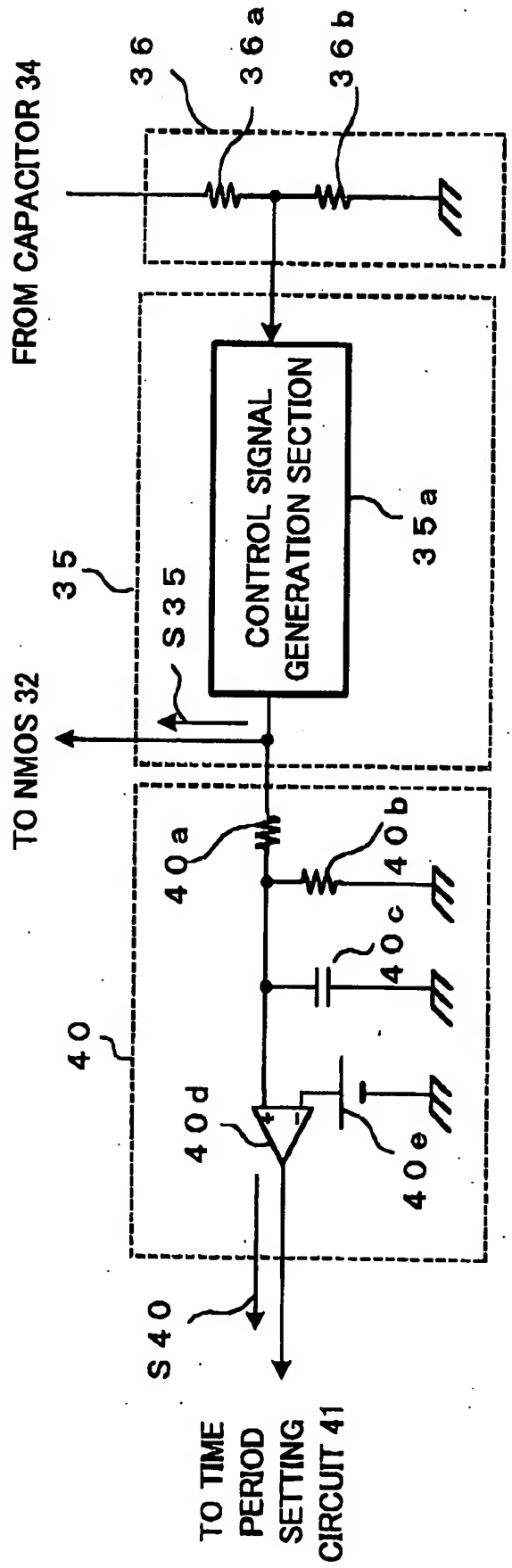
FROM CAPACITOR 34
36
36a
36b
CONTROL SIGNAL GENERATION SECTION
35a
35
S35
TO NMOS 32
40a
40b
40c
40
40d
40e
S40
TO TIME PERIOD SETTING CIRCUIT 41

FIG. 3

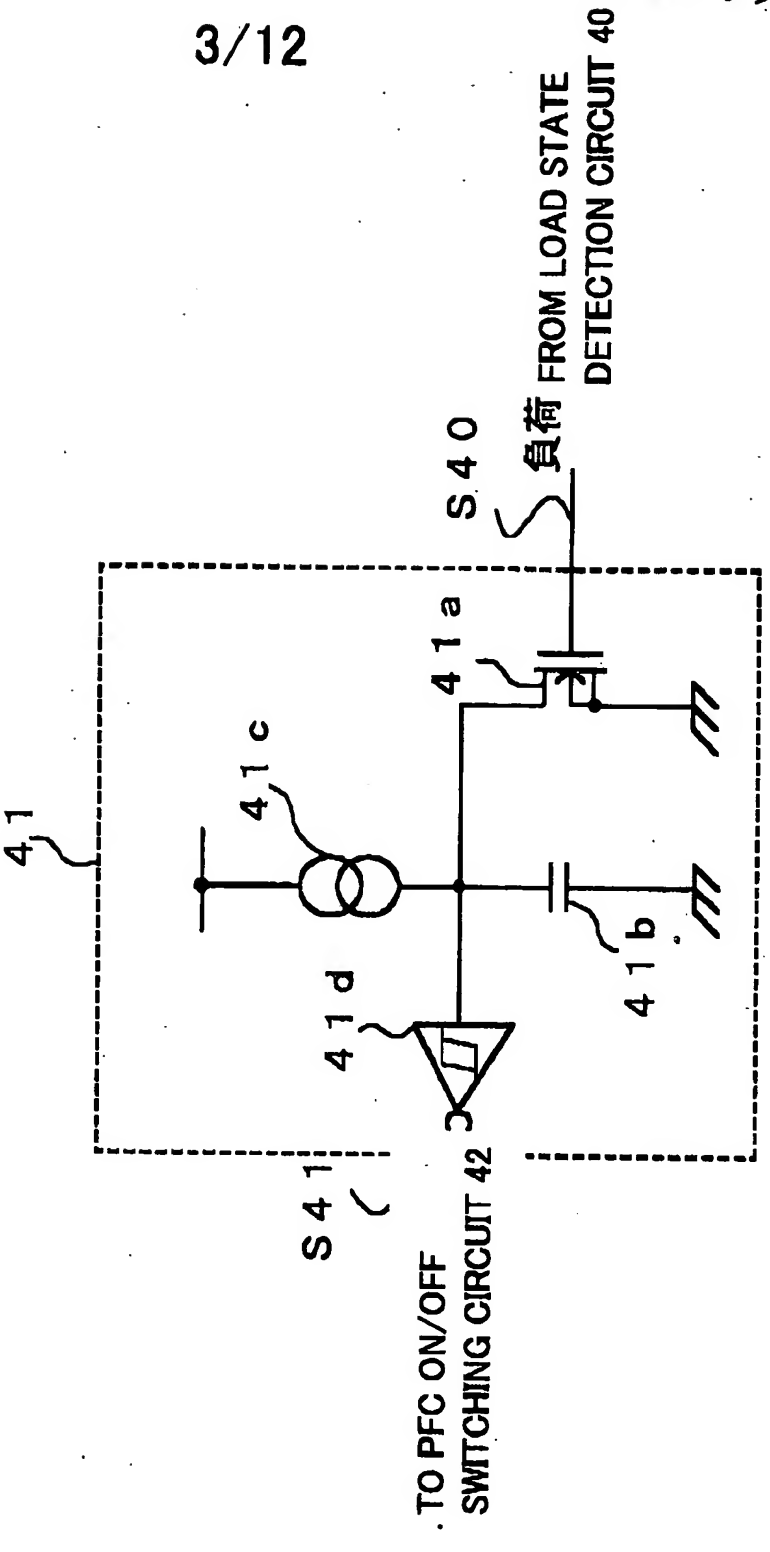
FROM LOAD STATE DETECTION CIRCUIT 40
負荷
S40
41a
41c
41
41b
41d
S41
TO PFC ON/OFF SWITCHING CIRCUIT 42
P

FIG.4

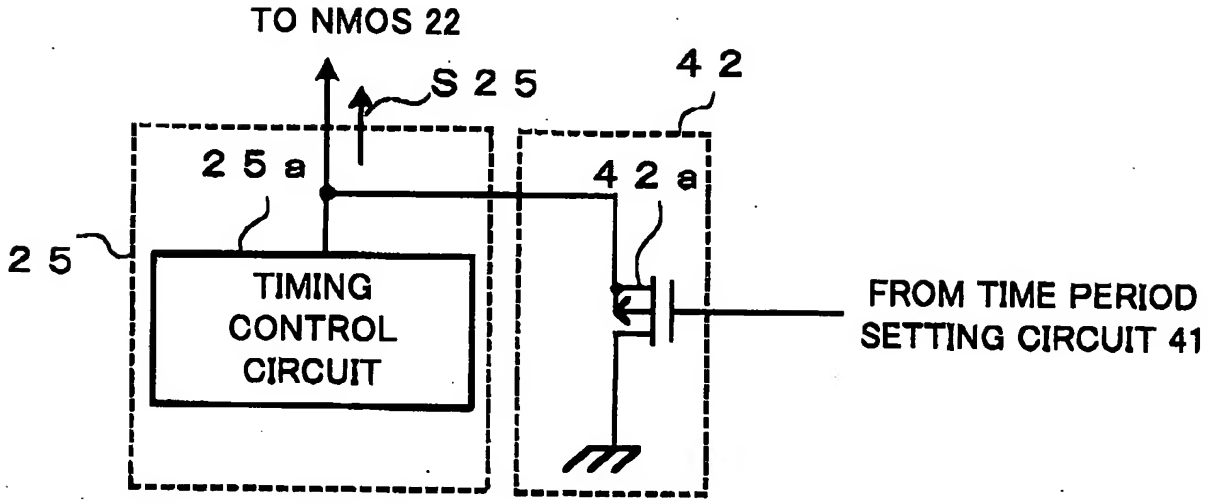
TO NMOS 22
S 2 5
4 2
2 5 a
4 2 a
2 5
TIMING CONTROL CIRCUIT
FROM TIME PERIOD SETTING CIRCUIT 41

FIG. 5

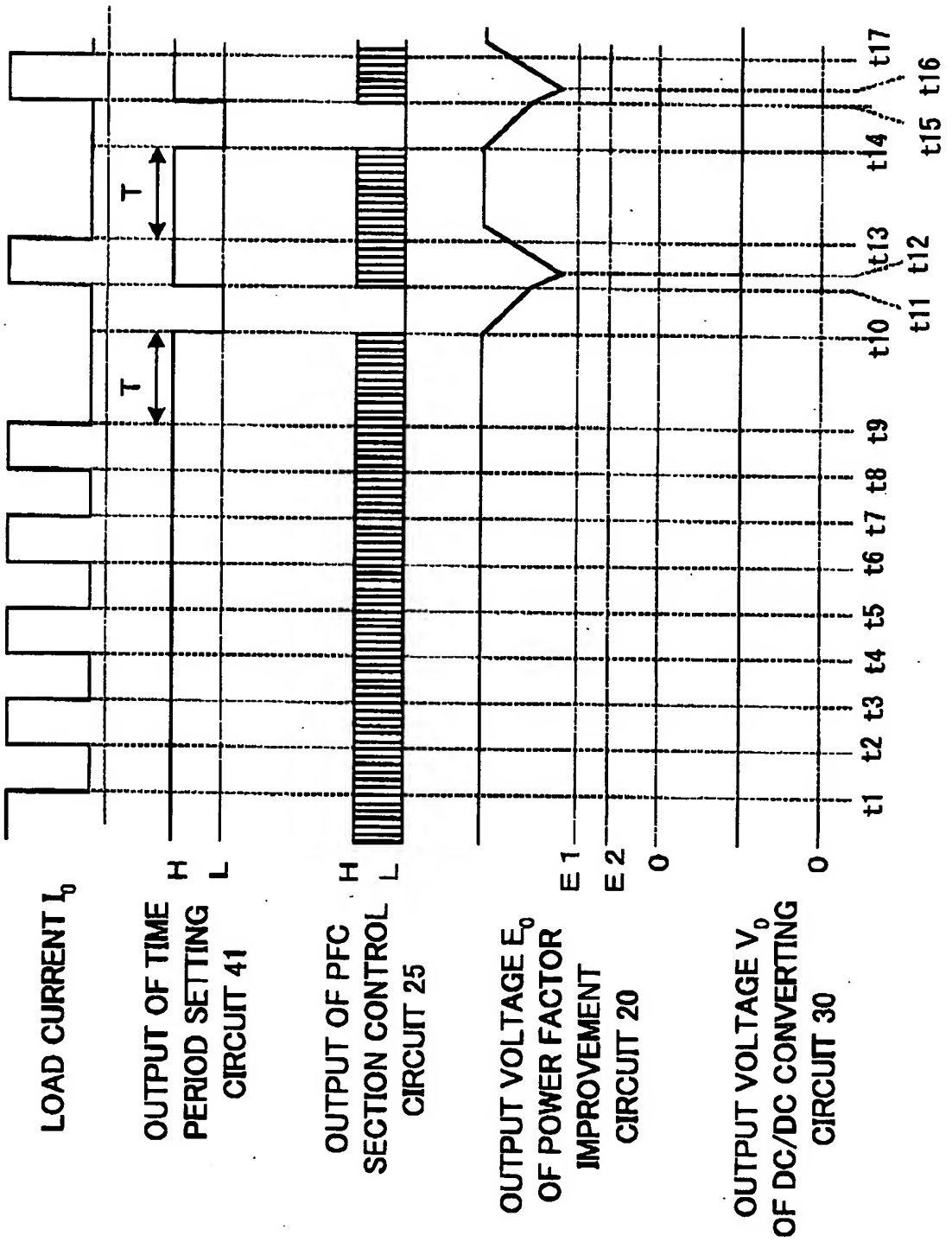
LOAD CURRENT I_0
OUTPUT OF TIME PERIOD SETTING CIRCUIT 41
OUTPUT OF PFC SECTION CONTROL CIRCUIT 25
OUTPUT VOLTAGE E_0 OF POWER FACTOR IMPROVEMENT CIRCUIT 20
OUTPUT VOLTAGE V_0 OF DC/DC CONVERTING CIRCUIT 30
H
L
T
T
E1
E2
0
0
t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17

FIG. 6

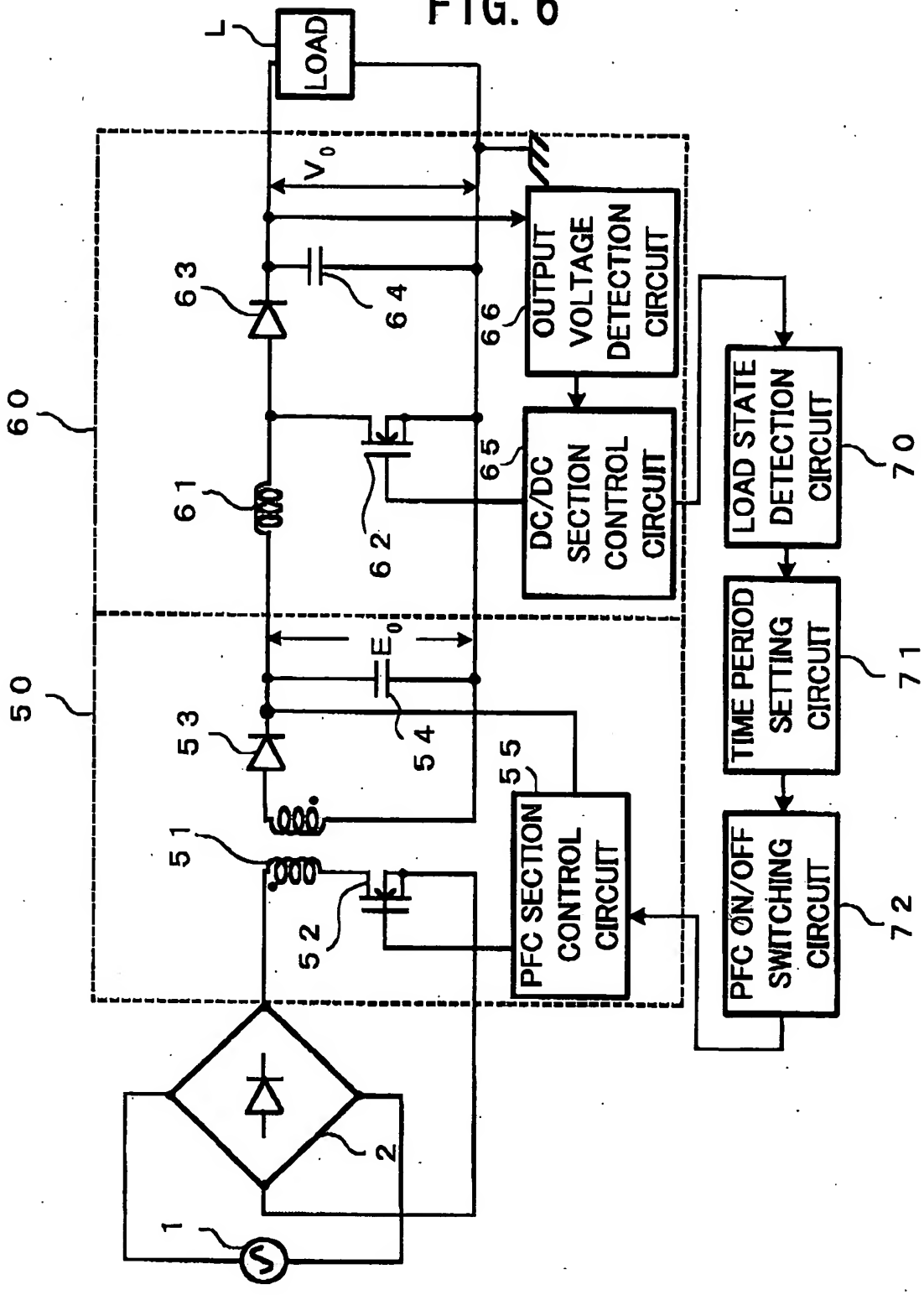

FIG. 7

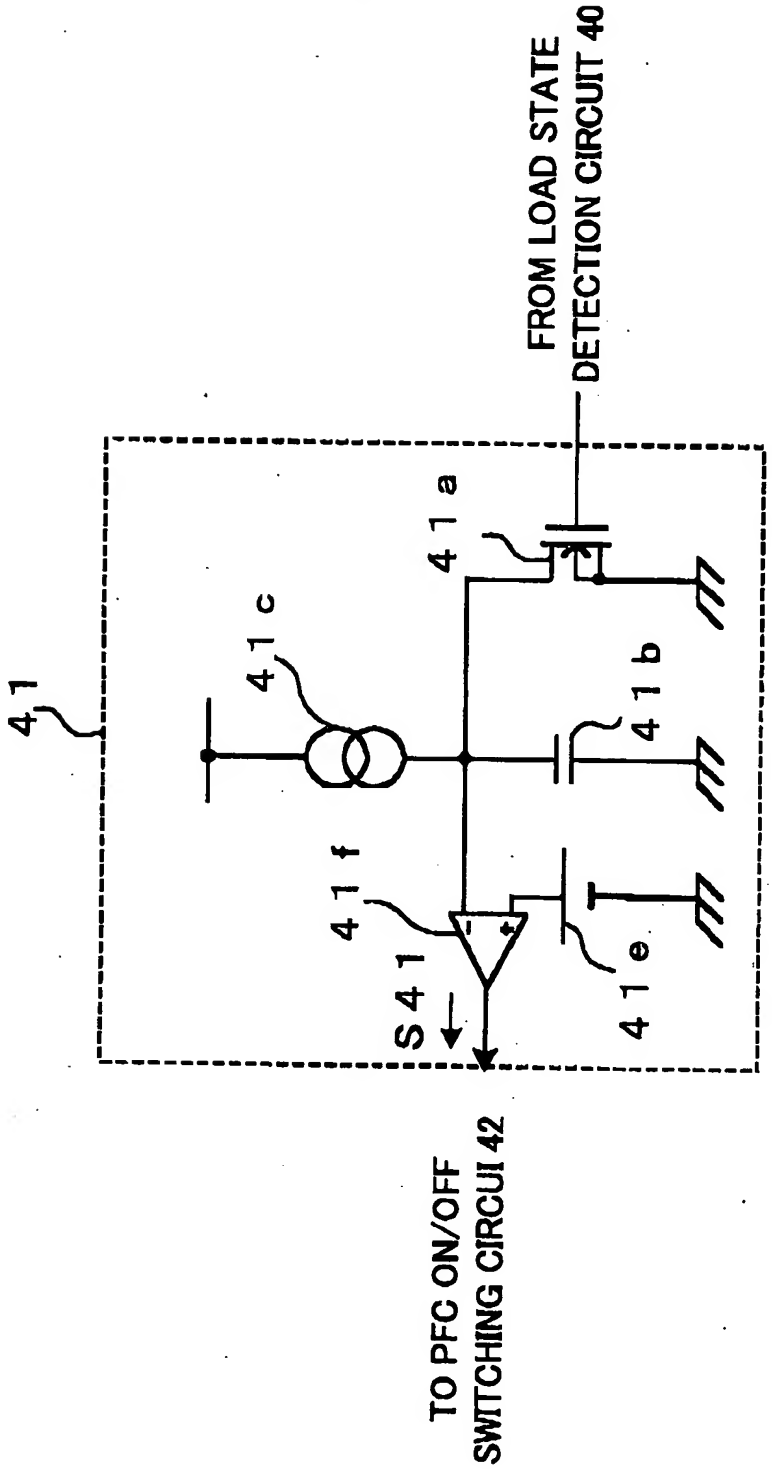
FROM LOAD STATE DETECTION CIRCUIT 40
41
41a
41b
41c
41e
41f
S41
TO PFC ON/OFF SWITCHING CIRCUI 42

FIG. 8

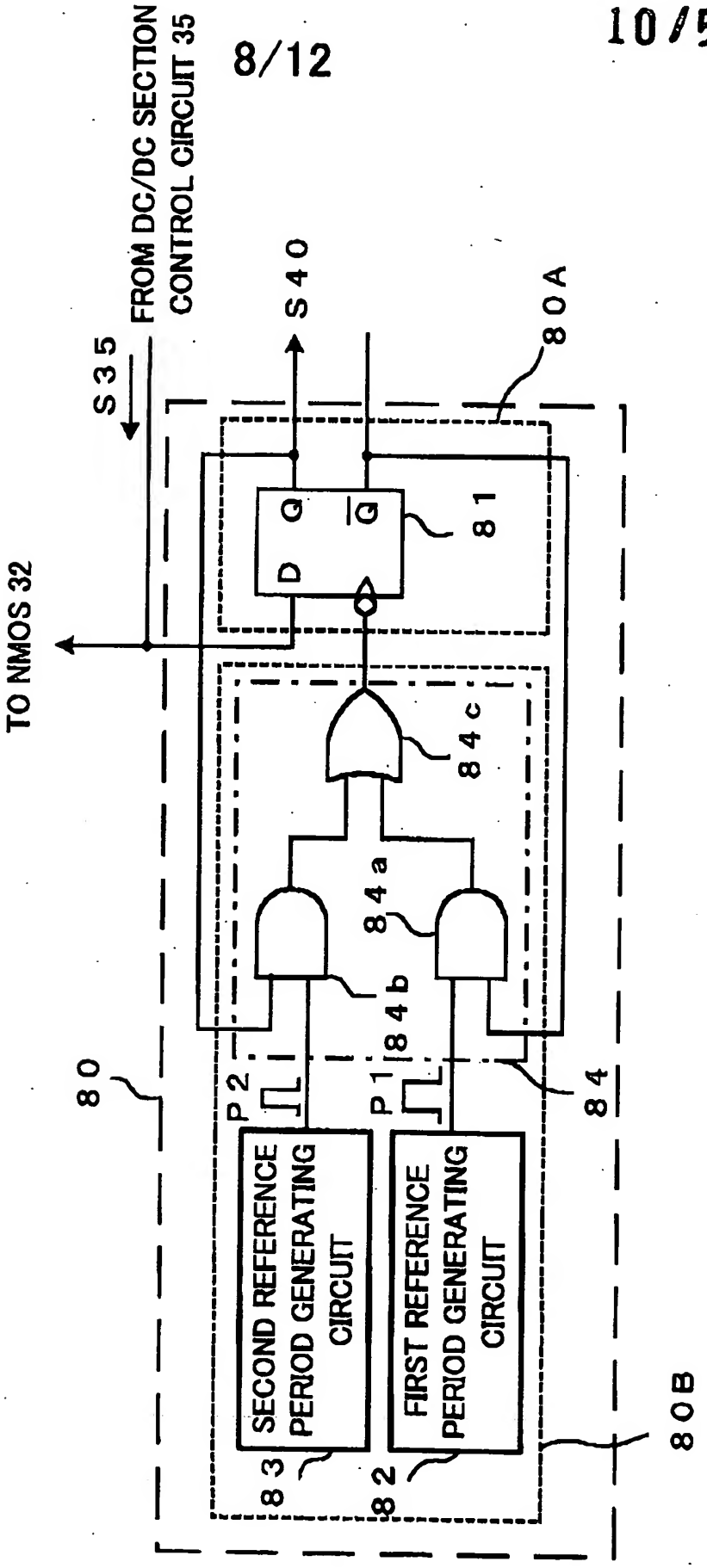
FROM DC/DC SECTION CONTROL CIRCUIT 35
S35
S40
80A
TO NMOS 32
D
Q
Q
81
84c
84a
84b
P2
P1
80
84
SECOND REFERENCE PERIOD GENERATING CIRCUIT
FIRST REFERENCE PERIOD GENERATING CIRCUIT
83
82
80B

FIG. 9

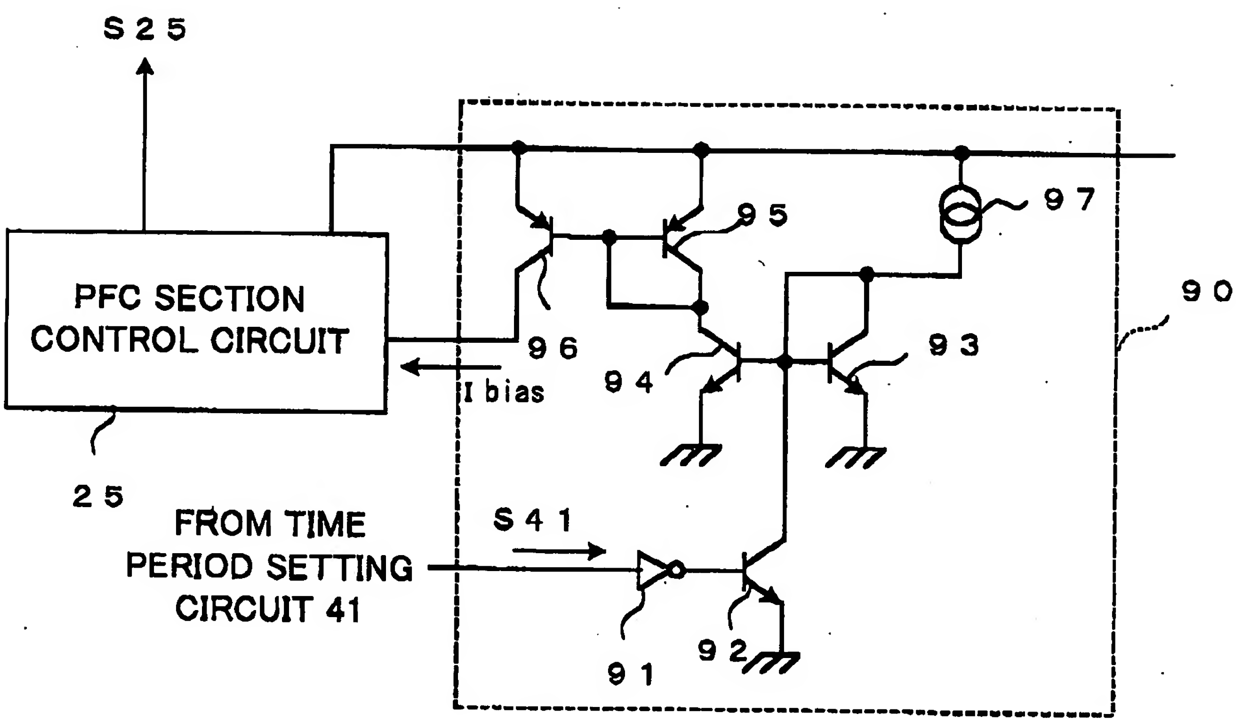
S25
PFC SECTION CONTROL CIRCUIT
25
I bias
FROM TIME PERIOD SETTING CIRCUIT 41
S41
91
92
93
94
95
96
97
90

FIG. 10

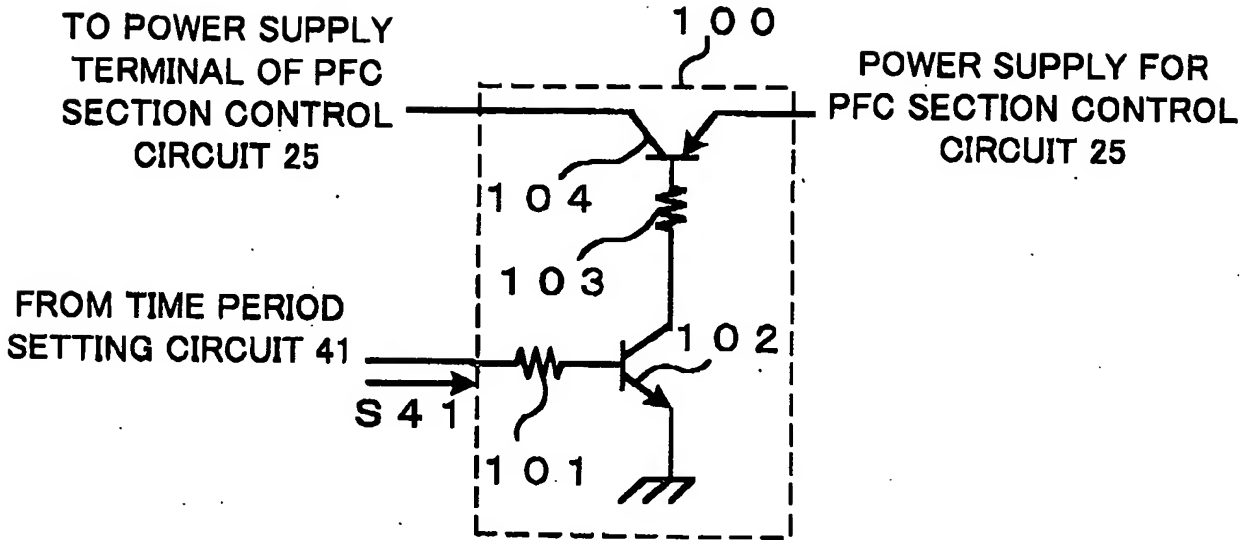
TO POWER SUPPLY TERMINAL OF PFC SECTION CONTROL CIRCUIT 25
100
POWER SUPPLY FOR PFC SECTION CONTROL CIRCUIT 25
104
103
FROM TIME PERIOD SETTING CIRCUIT 41
102
S41
101

FIG. 11

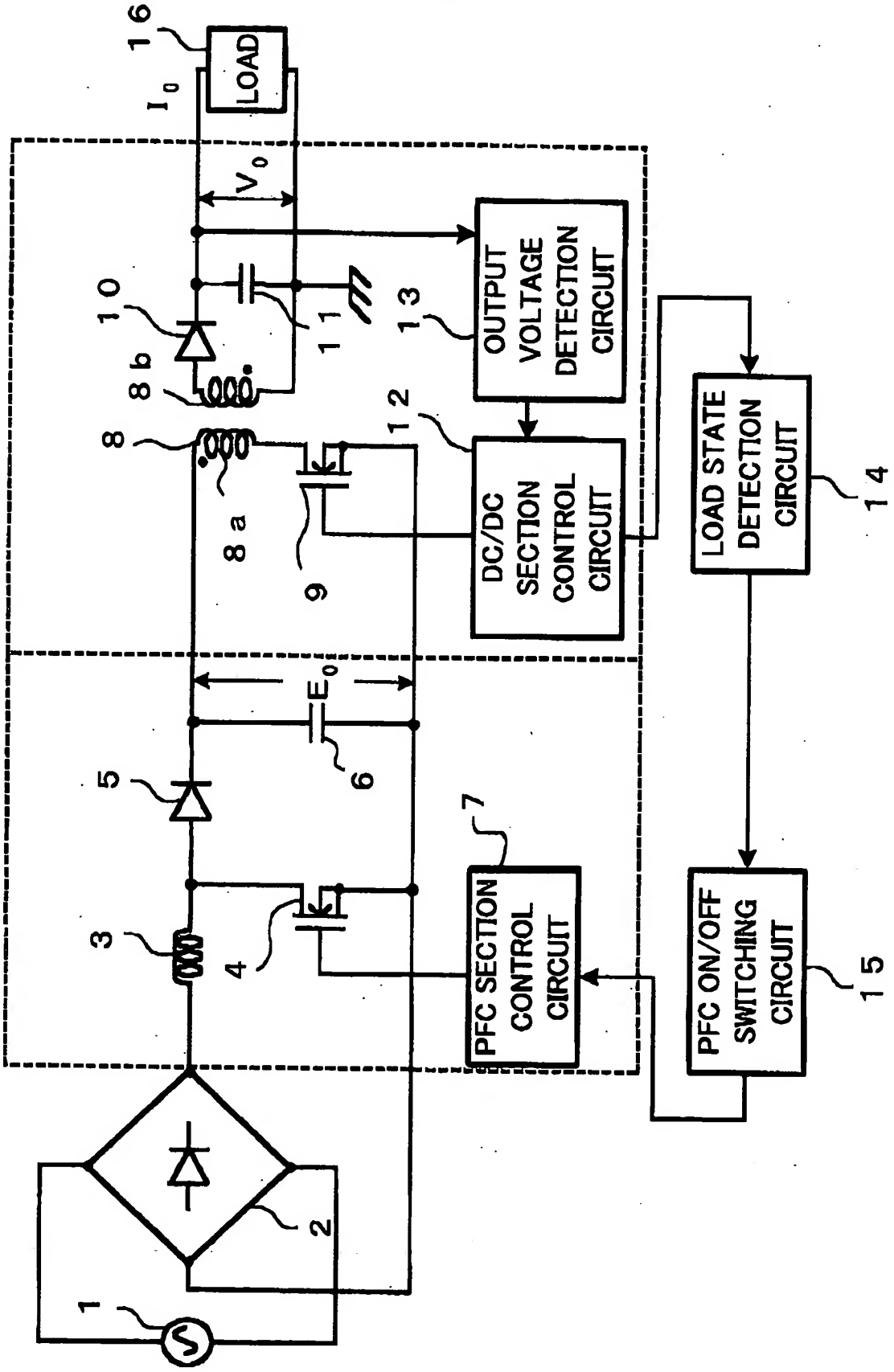
16
LOAD
I_0
V_0
OUTPUT VOLTAGE DETECTION CIRCUIT
13
10
11
8b
8
12
8a
9
DC/DC SECTION CONTROL CIRCUIT
LOAD STATE DETECTION CIRCUIT
14
E_0
6
5
7
3
4
PFC SECTION CONTROL CIRCUIT
PFC ON/OFF SWITCHING CIRCUIT
15
2
1
S

FIG. 12